In the Claims

Please replace all prior versions, and listings, of claims in the application with the following list of claims:

1. (Currently Amended) An electrical device comprising ~~a region having~~ at least four semiconductors assembled together as a component of the electrical device, each of the at least four semiconductors ~~being a free-standing and bulk-doped semiconductor~~ comprising at least one portion having a smallest width of less than 500 nanometers, wherein the at least four semiconductors have a variation in diameter of less than 20% and are made by a process of selecting a population of catalyst colloid particles having a variation in diameter of less than 20% and growing the population of semiconductors catalytically from the catalyst colloid particles, thereby producing the at least four semiconductors having a variation in diameter of less than 20%.

2. (Previously Presented) The device of claim 1, wherein the device includes at least one semiconductor comprising:

an interior core comprising a first semiconductor; and

one or more exterior shells exterior to the interior core, at least one of the exterior shells comprising a different material than the first semiconductor.

3. (Withdrawn) The semiconductor of claim 1, wherein the semiconductor comprises an elemental semiconductor.

4. (Withdrawn) The semiconductor of claim 3, wherein the elemental semiconductor is selected from a group consisting of: Si, Ge, Sn, Se, Te, B, Diamond and P.

5. (Previously Presented) The device of claim 1, wherein the device includes at least one semiconductor comprising a solid solution of elemental semiconductors.

6. (Previously Presented) The device of claim 5, wherein the solid solution is selected from a group consisting of: B-C, B-P(BP_6), B-Si, Si-C, Si-Ge, Si-Sn and Ge-Sn.

7. (Previously Presented) The device of claim 1, wherein the device includes at least one semiconductor comprising a Group IV-Group IV semiconductor.

8. (Previously Presented) The device of claim 7, wherein the Group IV-Group IV semiconductor is SiC.

9. (Withdrawn) The semiconductor of claim 1, wherein the semiconductor comprises a Group III-Group V semiconductor.

10. (Withdrawn) The semiconductor of claim 9, wherein the Group III-Group V semiconductor is selected from a group consisting of: BN/BP/BAs, AlN/AlP/AlAs/AlSb, GaN/GaP/GaAs/GaSb, InN/InP/InAs/InSb.

11. (Withdrawn) The semiconductor of claim 1, wherein the semiconductor comprises an alloy comprising a combination of two or more Group III-Group V semiconductors from a group consisting of: BN/BP/BAs, AlN/AlP/AlAs/AlSb, GaN/GaP/GaAs/GaSb, InN/InP/InAs/InSb.

12. (Withdrawn) The semiconductor of claim 1, wherein the semiconductor comprises a Group II-Group VI semiconductor.

13. (Withdrawn) The semiconductor of claim 12, wherein the semiconductor is selected from a group consisting of: ZnO/ZnS/ZnSe/ZnTe, CdS/CdSe/CdTe, HgS/HgSe/HgTe, BeS/BeSe/BeTe/MgS/MgSe.

14. (Withdrawn) The semiconductor of claim 1, wherein the semiconductor comprises an alloy comprising a combination of two or more Group II-Group VI semiconductors from a group consisting of: ZnO/ZnS/ZnSe/ZnTe, CdS/CdSe/CdTe, HgS/HgSe/HgTe, BeS/BeSe/BeTe/MgS/MgSe.

15. (Withdrawn) The semiconductor of claim 1, wherein the semiconductor comprises an alloy comprising a combination of a Group II-Group VI semiconductors from a group consisting of: ZnO/ZnS/ZnSe/ZnTe, CdS/CdSe/CdTe, HgS/HgSe/HgTe, BeS/BeSe/BeTe/MgS/MgSe and a Group III-Group V semiconductors from a group consisting of: BN/BP/BAs, AlN/AlP/AlAs/AlSb, GaN/GaP/GaAs/GaSb, InN/InP/InAs/InSb.

16. (Withdrawn) The semiconductor of claim 1, wherein the semiconductor comprises a Group IV-Group VI semiconductor.

17. (Withdrawn) The semiconductor of claim 16, wherein the semiconductor is selected from a group consisting of: GeS, GeSe, GeTe, SnS, SnSe, SnTe, PbO, PbS, PbSe, PbTe.

18. (Withdrawn) The semiconductor of claim 1, wherein the semiconductor comprises a Group I-Group VII semiconductor.

19. (Withdrawn) The semiconductor of claim 18, wherein the semiconductor is selected from a group consisting of: CuF, CuCl, CuBr, CuI, AgF, AgCl, AgBr, AgI.

20. (Withdrawn) The semiconductor of claim 1, wherein the semiconductor comprises a semiconductor selected from a group consisting of: BeSiN2, CaCN2, ZnGeP2, CdSnAs2, ZnSnSb2, CuGeP3, CuSi2P3, (Cu, Ag)(Al, Ga, In, Tl, Fe)(S, Se, Te)2, Si3N4, Ge3N4, Al2O3, (Al, Ga, In)2(S, Se, Te)3 and Al2CO.

21. (Withdrawn) The semiconductor of claim 1, wherein the semiconductor comprises a p-type dopant.

22. (Withdrawn) The semiconductor of claim 1, wherein the semiconductor comprises an n-type dopant from.

23. (Withdrawn) The semiconductor of claim 1, wherein the semiconductor comprises a p-type dopant from Group III of the periodic table.

24. (Withdrawn) The semiconductor of claim 1, wherein the semiconductor comprises an n-type dopant from Group V of the periodic table.

25. (Withdrawn) The semiconductor of claim 1, wherein the semiconductor comprises a p-type dopant selected from a group consisting of: B, Al and In.

26. (Withdrawn) The semiconductor of claim 1, wherein the semiconductor comprises an n-type dopant selected from a group consisting of: P, As and Sb.

27. (Withdrawn) The semiconductor of claim 1, wherein the semiconductor comprises a p-type dopant from Group II of the periodic table.

28. (Withdrawn) The semiconductor of claim 27, wherein the p-type dopant is selected from a group consisting of: Mg, Zn, Cd and Hg.

29. (Withdrawn) The semiconductor of claim 1, wherein the semiconductor comprises a p-type dopant from Group IV of the periodic table.

30. (Withdrawn) The semiconductor of claim 29, wherein the p-type dopant is selected from a group consisting of: C and Si.

31. (Withdrawn) The semiconductor of claim 27, wherein the n-type is selected from a group consisting of: Si, Ge, Sn, S, Se and Te.

32. (Previously Presented) The device of claim 1, wherein the smallest width is less than 200 nanometers.

33. (Previously Presented) The device of claim 1, wherein the smallest width is less than 150 nanometers.

34. (Previously Presented) The device of claim 1, wherein the smallest width is less than 100 nanometers.

35. (Previously Presented) The device of claim 1, wherein the smallest width is less than 80 nanometers.

36. (Previously Presented) The device of claim 1, wherein the smallest width is less than 70 nanometers.

37. (Previously Presented) The device of claim 1, wherein the smallest width is less than 60 nanometers.

38. (Previously Presented) The device of claim 1, wherein the smallest width is less than 40 nanometers.

39. (Previously Presented) The device of claim 1, wherein the smallest width is less than 20 nanometers.

40. (Previously Presented) The device of claim 1, wherein the smallest width is less than 10 nanometers.

41. (Previously Presented) The device of claim 1, wherein the smallest width is less than 5 nanometers.

42. (Previously Presented) The device of claim 1, wherein at least one of the at least four semiconductors is elongated, and the at least one portion of the at least one semiconductor is a longitudinal section.

43. (Previously Presented) The device of claim 42, wherein the longitudinal section has a ratio of the length of the section to a longest width greater than 4:1.

44. (Previously Presented) The device of claim 42, wherein the longitudinal section has a ratio of the length of the section to a longest width greater than 10:1.

45. (Previously Presented) The device of claim 42, wherein the longitudinal section has a ratio of the length of the section to a longest width greater than 100:1.

46. (Previously Presented) The device of claim 42, wherein the longitudinal section has a ratio of the length of the section to a longest width greater than 1000:1.

47. (Previously Presented) The device of claim 1, wherein the device includes at least one semiconductor comprising a single crystal.

48. (Cancelled)

49. (Withdrawn) The semiconductor of claim 1, wherein the semiconductor is n-doped.

50. (Withdrawn) The semiconductor of claim 1, wherein the semiconductor is p-doped.

51. (Withdrawn) The semiconductor of claim 1, wherein the semiconductor is magnetic.

52. (Withdrawn) The semiconductor of claim 51, wherein the semiconductor comprises a dopant making the semiconductor magnetic.

53. (Withdrawn) The semiconductor of claim 51, wherein the semiconductor is ferromagnetic.

54. (Withdrawn) The semiconductor of claim 53, wherein the semiconductor comprises a dopant that makes the semiconductor ferromagnetic.

55. (Withdrawn) The semiconductor of claim 54, wherein the semiconductor comprises manganese.

56. (Currently Amended) An electrical device comprising ~~a region having~~ at least four semiconductors assembled together as a component of the electrical device, each of the at least four semiconductors ~~being an elongated and bulk doped semiconductor~~ having a longitudinal axis such that, at any point along ~~its~~ the longitudinal axis, the semiconductor has a largest cross-sectional dimension less than 500 nanometers, wherein the at least four semiconductors have a variation in diameter of less than 20% and are made by a process of selecting a population of catalyst colloid particles having a variation in diameter of less than 20% and growing the population of semiconductors catalytically from the catalyst colloid particles, thereby producing the at least four semiconductors having a variation in diameter of less than 20%.

57. (Previously Presented) The device of claim 56, wherein the device includes at least one semiconductor comprising:

an interior core comprising a first semiconductor; and

one or more exterior shells exterior to the interior core, at least one of the exterior shells comprising a different material than the first semiconductor.

58. (Previously Presented) The device of claim 56, wherein, at any point along the longitudinal axis of at least one of the at least four semiconductors, a ratio of the length of the section to a longest width is greater than 4:1.

59. (Previously Presented) The device of claim 56, wherein, at any point along the longitudinal axis of at least one of the at least four semiconductors, a ratio of the length of the section to a longest width is greater than 10:1.

60. (Previously Presented) The device of claim 56, wherein, at any point along the longitudinal axis of at least one of the at least four semiconductors, a ratio of the length of the section to a longest width is greater than 100:1.

61. (Previously Presented) The device of claim 56, wherein, at any point along the longitudinal axis of at least one of the at least four semiconductors, a ratio of the length of the section to a longest width is greater than 1000:1.

62. (Previously Presented) The device of claim 56, wherein the point has a smallest width less than 200 nanometers.

63. (Previously Presented) The device of claim 56, wherein the point has a smallest width less than 150 nanometers.

64. (Previously Presented) The device of claim 56, wherein the point has a smallest width less than 100 nanometers.

65. (Previously Presented) The device of claim 56, wherein the point has a smallest width less than 80 nanometers.

66. (Previously Presented) The device of claim 56, wherein the point has a smallest width less than 70 nanometers.

67. (Previously Presented) The device of claim 56, wherein the point has a smallest width less than 60 nanometers.

68. (Previously Presented) The device of claim 56, wherein the point has a smallest width less than 40 nanometers.

69. (Previously Presented) The device of claim 56, wherein the point has a smallest width less than 20 nanometers.

70. (Previously Presented) The device of claim 56, wherein the point has a smallest width less than 10 nanometers.

71. (Previously Presented) The device of claim 56, wherein the point has a smallest width less than 5 nanometers.

72. (Previously Presented) The device of claim 56, wherein the device includes at least one semiconductor comprising a single crystal.

73-74. (Cancelled)

75. (Previously Presented) The device of claim 56, wherein the device includes at least one semiconductor that is n-doped.

76. (Previously Presented) The device of claim 56, wherein the device includes at least one semiconductor that is p-doped.

77-96. (Cancelled)

97. (Currently Amended) An electrical device comprising ~~a region having~~ at least four ~~bulk doped~~ semiconductors assembled together as a component of the electrical device, each of the at least four semiconductors having a variation in diameter of less than 20%, each of the at least four semiconductors independently being at least one of the following: a single crystal, an elongated ~~and bulk doped~~ semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a ~~free-standing and bulk doped~~ semiconductor with at least one portion having a smallest width of less than 500 nanometers, wherein a phenomena produced by a section of the ~~bulk doped~~ semiconductor exhibits a quantum confinement caused by a dimension of the section, and wherein the at least four semiconductors are made by a process of selecting a population of catalyst colloid particles having a variation in diameter of less than 20% and growing the population of semiconductors catalytically from the catalyst colloid particles, thereby producing the at least four semiconductors having a variation in diameter of less than 20%.

98. (Previously Presented) The device of claim 97, wherein at least one of the at least four semiconductors is elongated, and the dimension of the at least one semiconductor is a width at any point along a longitudinal section of the semiconductor.

99. (Previously Presented) The device of claim 98, wherein the longitudinal section is capable of transporting electrical carriers without scattering.

100. (Previously Presented) The device of claim 99, wherein the longitudinal section is capable of transporting electrical carriers such that the electrical carriers pass through the longitudinal section ballistically.

101. (Previously Presented) The device of claim 99, wherein the longitudinal section is capable of transporting electrical carriers such that the electrical carriers pass through the longitudinal section coherently.

102. (Withdrawn) The semiconductor of claim 98, wherein the longitudinal section is capable of transporting electrical carriers such that the electrical carriers are spin-polarized.

103. (Withdrawn) The semiconductor of claim 102, wherein the longitudinal section is capable of transporting electrical carriers such that the spin-polarized electrical carriers pass through the longitudinal section without losing spin information.

104. (Withdrawn) The semiconductor of claim 98, wherein the longitudinal section is capable of emitting light in response to excitation, wherein a wavelength of the emitted light is related to the width.

105. (Withdrawn) The semiconductor of claim 99, wherein the wavelength of the emitted light is proportional to the width.

106. (Currently Amended) A device comprising a region having at least four ~~bulk doped~~ semiconductors that each exhibit coherent transport, wherein the at least four semiconductors

have a variation in diameter of less than 20%, and wherein the at least four semiconductors are made by a process of selecting a population of catalyst colloid particles having a variation in diameter of less than 20% and growing the population of semiconductors catalytically from the catalyst colloid particles, thereby producing the at least four semiconductors having a variation in diameter of less than 20%.

107. (Currently Amended) A device comprising a region having at least four ~~bulk-doped~~ semiconductors that each exhibit ballistic transport, wherein the at least four semiconductors have a variation in diameter of less than 20%, and wherein the at least four semiconductors are made by a process of selecting a population of catalyst colloid particles having a variation in diameter of less than 20% and growing the population of semiconductors catalytically from the catalyst colloid particles, thereby producing the at least four semiconductors having a variation in diameter of less than 20%.

108. (Currently Amended) A device, comprising a region having at least four ~~bulk-doped~~ semiconductors that each exhibit Luttinger liquid behavior, wherein the at least four semiconductors have a variation in diameter of less than 20%, and wherein the at least four semiconductors are made by a process of selecting a population of catalyst colloid particles having a variation in diameter of less than 20% and growing the population of semiconductors catalytically from the catalyst colloid particles, thereby producing the at least four semiconductors having a variation in diameter of less than 20%.

109. (Withdrawn) A solution comprising one or more doped semiconductors, wherein at least one of the semiconductors is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers.

110. (Currently Amended) An electrical device comprising ~~a region having~~ at least four doped semiconductors assembled together as a component of the electrical device, the at least four doped semiconductors having a variation in diameter of less than 20%, wherein each of the

at least four doped semiconductors is independently at least one of the following: a single crystal, an elongated ~~and bulk-doped~~ semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a ~~free-standing and bulk-doped~~ semiconductor with at least one portion having a smallest width of less than 500 nanometers, wherein the at least four semiconductors are made by a process of selecting a population of catalyst colloid particles having a variation in diameter of less than 20% and growing the population of semiconductors catalytically from the catalyst colloid particles, thereby producing the at least four semiconductors having a variation in diameter of less than 20%.

111. (Withdrawn) The device of claim 110, wherein the device comprises at least two doped semiconductors, wherein both of the at least two doped semiconductors is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers, and wherein a first of the at least two doped semiconductors exhibits quantum confinement and a second of the at least two doped semiconductor manipulates the quantum confinement of the first.

112. (Cancelled)

113. (Withdrawn) The device of claim 111, wherein the at least two bulk-doped semiconductors are in physical contact with each other.

114. (Withdrawn) The device of claim 113, wherein a first of the at least two bulk-doped semiconductors is of a first conductivity type, and a second of the at least two bulk-doped semiconductors is of a second conductivity type.

115. (Withdrawn) The device of claim 114, wherein the first conductivity type is n-type, and the second type of conductivity type is p-type.

116. (Withdrawn) The device of claim 115, wherein the at least two bulk-doped semiconductors form a p-n junction.

117. (Cancelled)

118. (Previously Presented) The device of claim 110, wherein the device includes at least one semiconductor that is elongated.

119. (Previously Presented) The device of claim 110, wherein the device includes at least one semiconductor comprising a single crystal.

120. (Previously Presented) The device of claim 110, wherein the device includes at least one semiconductor comprising:

an interior core comprising a first semiconductor; and

an exterior shell comprising a different material than the first semiconductor.

121. (Withdrawn) The device of claim 110, wherein the device comprises a switch.

122. (Withdrawn) The device of claim 110, wherein the device comprises a diode.

123. (Withdrawn) The device of claim 110, wherein the device comprises a Light-Emitting.

124. (Withdrawn) The device of claim 110, wherein the device comprises a tunnel diode.

125. (Withdrawn) The device of claim 110, wherein the device comprises a Schottky diode.

126. (Withdrawn) The device of claim 125, wherein the transistor comprises a Bipolar Junction Transistor.

127. (Withdrawn) The device of claim 125, wherein the transistor comprises a Field Effect Transistor.

128. (Withdrawn) The device of claim 110, wherein the device comprises an inverter.

129. (Withdrawn) The device of claim 128, wherein the inverter is a complimentary inverter.

130. (Withdrawn) The device of claim 110, wherein the device comprises an optical sensor.

131. (Withdrawn) The device of claim 110, wherein the device comprises a sensor for an analyte.

132. (Withdrawn) The device of claim 110, wherein the analyte is a DNA.

133. (Withdrawn) The device of claim 110, wherein the device comprises a memory device.

134. (Withdrawn) The device of claim 133, wherein the memory device is a dynamic memory device.

135. (Withdrawn) The device of claim 133, wherein the memory device is a static memory device.

136. (Withdrawn) The device of claim 110, wherein the device comprises a laser.

137. (Withdrawn) The device of claim 110, wherein the device comprises a logic gate.

138. (Withdrawn) The device of claim 137, wherein the logic gate is an AND gate.

139. (Withdrawn) The device of claim 137, wherein the logic gate is a NAND gate.

140. (Withdrawn) The device of claim 137, wherein the logic gate is an EXCLUSIVE-AND gate.

141. (Withdrawn) The device of claim 137, wherein the logic gate is a OR gate.

142. (Withdrawn) The device of claim 137, wherein the logic gate is a NOR gate.

143. (Withdrawn) The device of claim 137, wherein the logic gate is an EXCLUSIVE-OR gate.

144. (Withdrawn) The device of claim 110, wherein the device comprises a latch.

145. (Withdrawn) The device of claim 110, wherein the device comprises a register.

146. (Withdrawn) The device of claim 110, wherein the device comprises clock circuitry.

147. (Withdrawn) The device of claim 110, wherein the device comprises a logic array.

148. (Withdrawn) The device of claim 110, wherein the device comprises a state machine.

149. (Withdrawn) The device of claim 110, wherein the device comprises a programmable circuit.

150. (Withdrawn) The device of claim 110, wherein the device comprises an amplifier.

151. (Withdrawn) The device of claim 110, wherein the device comprises a transformer.

152. (Withdrawn) The device of claim 110, wherein the device comprises a signal processor.

153. (Withdrawn) The device of claim 110, wherein the device comprises a digital circuit.

154. (Withdrawn) The device of claim 110, wherein the device comprises an analog circuit.

155. (Withdrawn) The device of claim 110, wherein the device comprises a light emission source.

156. (Withdrawn) The device of claim 155, wherein the light emission source emits light at a higher frequency than would the semiconductor if the semiconductor had a shortest width greater than the shortest width at any portion of the semiconductor.

157. (Withdrawn) The device of claim 110, wherein the device comprises a photoluminescent device.

158. (Withdrawn) The device of claim 110, wherein the device comprises an electroluminescent device.

159. (Withdrawn) The device of claim 110, wherein the device comprises a rectifier.

160. (Withdrawn) The device of claim 110, wherein the device comprises a photodiode.

161. (Withdrawn) The device of claim 110, wherein the device comprises a p-n solar cell.

162. (Withdrawn) The device of claim 110, wherein the device comprises a phototransistor.

163. (Withdrawn) The device of claim 110, wherein the device comprises a single-electron transistor.

164. (Withdrawn) The device of claim 110, wherein the device comprises a single photon emitter.

165. (Withdrawn) The device of claim 110, wherein the device comprises a single photon detector.

166. (Withdrawn) The device of claim 110, wherein the device comprises a spintronic device.

167. (Withdrawn) The device of claim 110, wherein the device comprises an ultra-sharp tip for atomic force microscope.

168. (Withdrawn) The device of claim 110, wherein the device comprises a scanning tunneling microscope.

169. (Withdrawn) The device of claim, wherein the device comprises a field emission device

170. (Withdrawn) The device of claim, wherein the device comprises a photoluminescence tag

171. (Withdrawn) The device of claim, wherein the device comprises a photovoltaic device.

172. (Withdrawn) The device of claim, wherein the device comprises photonic band gap materials.

173. (Withdrawn) The device of claim 110, wherein the device comprises a scanning near field optical microscope tips.

174. (Withdrawn) The device of claim 110, wherein the device comprises a circuit that has digital and analog components.

175. (Previously Presented) The device of claim 110, wherein the device comprises another semiconductor that is electrically coupled to at least one of the at least four doped semiconductors.

176. (Withdrawn) The device of claim 175, wherein the other semiconductor is a bulk-doped semiconductor comprising at least one portion having a smallest width of less than 500 nanometers.

177. (Withdrawn) The device of claim 110, wherein the device comprises another semiconductor that is optically coupled to the at least one bulk-doped semiconductor.

178. (Withdrawn) The device of claim 177, wherein the other semiconductor is a bulk-doped semiconductor comprising at least one portion having a smallest width of less than 500 nanometers.

179. (Withdrawn) The device of claim 110, wherein the device comprises another semiconductor that is magnetically coupled to the at least one bulk-doped semiconductor.

180. (Withdrawn) The device of claim 179, wherein the other semiconductor is a bulk-doped semiconductor comprising at least one portion having a smallest width of less than 500 nanometers.

181. (Previously Presented) The device of claim 110, wherein the device comprises another semiconductor that physically contacts at least one of the at least four doped semiconductors.

182. (Withdrawn) The device of claim 179, wherein the other semiconductor is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers.

183. (Previously Presented) The device of claim 110, wherein the device includes at least one semiconductor that is coupled to an electrical contact.

184. (Withdrawn) The device of claim 110, wherein the at least one semiconductor is coupled to an optical contact.

185. (Withdrawn) The device of claim 110, wherein the at least one semiconductor is coupled to a magnetic contact.

186. (Previously Presented) The device of claim 110, wherein a conductivity of at least one of the at least four semiconductors is controllable in response to a signal.

187. (Original) The device of claim 186, wherein the conductivity of the at least one semiconductor is controllable to have any value within a range of values.

188. (Original) The device of claim 186, wherein the at least one semiconductor is switchable between two or more states.

189. (Original) The device of claim 188, wherein the at least one semiconductor is switchable between a conducting state and an insulating state by the signal.

190. (Withdrawn) The device of claim 188, wherein two or more states of the at least one semiconductor are maintainable without an applied signal.

191. (Original) The device of claim 186, wherein the conductivity of the at least one semiconductor is controllable in response to an electrical signal.

192. (Withdrawn) The device of claim 186, wherein the conductivity of the at least one semiconductor is controllable in response to an optical signal.

193. (Withdrawn) The device of claim 186, wherein the conductivity of the at least one semiconductor is controllable in response to a magnetic signal.

194. (Previously Presented) The device of claim 186, wherein the conductivity of the at least one semiconductor is controllable in response to a signal of a gate terminal.

195. (Original) The device of claim 194, wherein the gate terminal is not in physical contact with the at least one semiconductor.

196. (Withdrawn) The device of claim 110, wherein at least two of the semiconductors form an array, and at least one of the semiconductors in the array is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers.

197. (Withdrawn) The device of claim 196, wherein the array is an ordered array.

198. (Withdrawn) The device of claim 196, wherein said array is not an ordered array.

199. (Withdrawn) The device of claim 110, wherein the device comprises two or more separate and interconnected circuits, at least one of the circuits not comprising a doped semiconductor that is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers.

200. (Withdrawn) The device of claim 110, wherein the device is embodied on a chip having one or more pinouts.

201. (Withdrawn) The device of claim 200, wherein the chip comprises separate and interconnected circuits, at least one of the circuits not comprising a doped semiconductor that is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers.

202-260. (Cancelled)

261. (Withdrawn) A semiconductor device, comprising

a silicon substrate having an array of metal contacts

a crossbar switch element formed in electrical communication with the array and having a first bar formed of a p-type semiconductor nanowire, and

a second bar formed of an n-type semiconductor nanowire and being spaced away from the first bar and being disposed transversely thereto.

262. (Withdrawn) A semi device of claim 261, wherein the second bar is spaces between 1-10 nm from the first bar.

263-333. (Cancelled)

334. (Previously Presented) A method, comprising:

growing a population of semiconductor nanowires, each having at least one portion having a smallest width less than 500 nanometers, catalytically from catalyst colloid particles selected such that the population of semiconductor nanowires produced according to the method has a variation in diameter of less than 20%.

335. (Previously Presented) The method of claim 334, wherein the catalyst colloid particles have a variation in diameter of less than about 20%.

336. (Previously Presented) The method of claim 334, comprising doping the population of semiconductor nanowires while growing the semiconductor nanowires to produce a population of doped semiconductor nanowires.

337. (Previously Presented) The method of claim 336, further comprising adding one or more other materials to a surface of at least some of the doped semiconductor nanowires.

338. (Previously Presented) The method of claim 337, comprising adding said one or more other materials to form a shell around the at least some of the doped semiconductor nanowires.

339. (Previously Presented) The method of claim 334, comprising growing the population of semiconductor nanowires using laser-assisted catalytic growth.

340. (Previously Presented) The method of claim 334, further comprising controlling the lengths of the population of semiconductor nanowires.

341. (Previously Presented) The method of claim 334, wherein at least a portion of the semiconductor nanowires has at least one portion having a smallest width of less than 20 nanometers.

342. (Previously Presented) The method of claim 334, wherein at least a portion of the semiconductor nanowires has at least one portion having a smallest width of less than 10 nanometers.

343. (Previously Presented) The method of claim 334, wherein at least a portion of the semiconductor nanowires has at least one portion having a smallest width of less than 5 nanometers.

344. (Previously Presented) The method of claim 334, wherein the catalyst colloid particles are size-selected by dilution.

345. (Previously Presented) The method of claim 334, further comprising depositing one or more semiconductor nanowires on a surface.

346. (Previously Presented) The method of claim 345, wherein the surface is a surface of a substrate.

347. (Previously Presented) The method of claim 345, wherein the depositing comprises contacting a solution comprising the one or more semiconductor nanowires to the surface.

348. (Previously Presented) The method of claim 347, further comprising aligning the one or more semiconductor nanowires on the surface.

349. (Previously Presented) The method of claim 348, wherein said aligning comprises orienting said one or more semiconductor nanowires using an electric field.

350. (Previously Presented) The method of claim 349, wherein said aligning comprises generating an electric field between at least two electrodes, and positioning the one or more semiconductor nanowires between the electrodes.

351. (Previously Presented) The method of claim 348, wherein said aligning comprising orienting the one or more semiconductor nanowires by applying a mechanical tool.

352. (Previously Presented) The method of claim 348, wherein said aligning comprises orienting said one or more semiconductor nanowires using a fluid flow.

353. (Previously Presented) The method of claim 352, wherein said aligning comprises flowing a fluid that comprises the one or more semiconductor nanowires onto the surface.

354. (Previously Presented) The method of claim 345, further comprising conditioning the surface to attach the one or more semiconductor nanowires to the surface.

355. (Previously Presented) The method of claim 354, wherein said conditioning comprises patterning the surface.

356. (Previously Presented) The method of claim 354, wherein said conditioning comprises functionalizing the surface with one or more functional groups which have an affinity for the semiconductor nanowires.

357. (Previously Presented) The method of claim 356, wherein the one or more functional groups comprises one or more alkyloxysilane groups.

358. (Previously Presented) The method of claim 345, comprising depositing the semiconductor nanowires on the surface to form a field-effect transistor.

359. (Previously Presented) The method of claim 345, comprising depositing the semiconductor nanowires on the surface to form a device comprising one or more than one of a switch, a diode, a light-emitting diode, a tunnel diode, a Schottky diode, a Bipolar Junction Transistor, an inverter, an optical sensor, a sensor for an analyte, a memory device, a laser, a logic gate, a latch, a register, an amplifier, a signal processor, a digital or analog circuit, a light emission source, a photodiode, a phototransistor, a photovoltaic device, or combinations thereof.

360. (Previously Presented) The method of claim 334, wherein at least some of the catalyst colloid particles comprises gold.

361. (Previously Presented) The method of claim 334, wherein at least some of the catalyst colloid particles each independently comprises one or more than one of Ag, Au, Cu, Zn, Cd, Fe, Ni, Co or mixtures thereof.

362. (Previously Presented) A method comprising making a semiconductor nanowire junction by crossing at least one p-type semiconductor nanowire with at least one n-type semiconductor nanowire, wherein one or both of the p-type semiconductor nanowire and the n-type semiconductor nanowire are chosen from a population of semiconductor nanowires grown according to the method of claim 334.

363. (Previously Presented) The method of claim 334, wherein the population of semiconductor nanowires have a variation in diameter of less than about 10%.

364. (Previously Presented) A method, comprising:

growing a population of semiconductor nanowires, each having at least one portion having a smallest width less than 500 nanometers, catalytically from catalyst colloid particles

pre-selected to minimize aggregation and to have substantially uniform size selected such that at least four of the semiconductor nanowires have a variation in diameter of less than 20%.

365. (Previously Presented) The method of claim 364, wherein the grown semiconductor nanowires have a variation in diameter of less than about 10%.

366. (Previously Presented) The method of claim 364, wherein the catalyst colloid particles have a variation in diameter of less than about 20%.

367. (Previously Presented) The method of claim 364, wherein the catalyst colloid particles are pre-selected by dilution.

368. (Previously Presented) A method, comprising:

growing a population of semiconductor nanowires, each having at least one portion having a smallest width less than 500 nanometers, from size-selected catalyst colloid particles.

369. (Previously Presented) The method of claim 368, wherein the catalyst colloid particles are size-selected to have a variation in diameter of less than about 20%.

370. (Previously Presented) The method of claim 368, wherein the catalyst colloid particles are size-selected to have a variation in diameter of less than about 10%.

371. (Previously Presented) The method of claim 368, wherein the catalyst colloid particles are size-selected by dilution.

372. (Previously Presented) The method of claim 368, comprising growing the population of semiconductor nanowires using laser-assisted catalytic growth.

373. (Previously Presented) A method of fabricating a semiconductor nanowire device comprising a region having at least four semiconductor nanowires, the method comprising growing the at least four semiconductor nanowires having a variation in diameter of less than

20%, and depositing the at least four grown semiconductor nanowires on a surface of a region of a device substrate.

374. (Previously Presented) A device comprising:

a substrate including a region having at least four semiconductor nanowires deposited thereon each comprising at least one portion having a smallest width less than 500 nanometers, the at least four semiconductor nanowires having a variation in diameter of less than about 20%.

375. (Previously Presented) The device of claim 374, wherein the semiconductor nanowires are deposited from solution onto the substrate.

376. (Previously Presented) The device of claim 374, wherein the at least four semiconductor nanowires have a variation in diameter of less than 10%.

377. (Previously Presented) The device of claim 374, wherein the at least four semiconductor nanowires are grown from size-selected catalyst colloid particles.

378. (Previously Presented) A method of growing a semiconductor, the method comprising an act of:

(A) doping the semiconductor during growth of the semiconductor.

379. (Previously Presented) The method of claim 378, wherein the grown semiconductor is a doped semiconductor that is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers.

380. (Previously Presented) The method of claim 378, further comprising an act of:

(B) adding one or more other materials to a surface of the doped semiconductor.

381. (Previously Presented) The method of claim 380, wherein act (B) comprises forming a shell around the doped semiconductor.

382. (Previously Presented) The method of claim 378, wherein act (A) comprises:
controlling an extent of the doping.

383. (Previously Presented) The method of claim 378, wherein act (A) comprises growing the doped semiconductor by applying energy to a collection of molecules, the collection of molecules comprising molecules of the semiconductor and molecules of a dopant.

384. (Previously Presented) The method of claim 383, wherein act (A) comprises an act of:
controlling an extent of the doping.

385. (Previously Presented) The method of claim 384, wherein the act of controlling doping comprises controlling a ratio of an amount of the semiconductor molecules to an amount of the dopant molecules.

386. (Previously Presented) The method of claim 384, wherein act (A) further comprises:
vaporizing the molecules using a laser to form vaporized molecules.

387. (Previously Presented) The method of claim 386, wherein act (A) further comprises:
growing the semiconductor from the vaporized molecules.

388. (Previously Presented) The method of claim 386, wherein act (A) further comprises:
condensing the vaporized molecules into a liquid cluster.

389. (Previously Presented) The method of claim 387, wherein act (A) further comprises:
growing the semiconductor from the liquid cluster.

390. (Previously Presented) The method of claim 386, wherein act (A) is performed using laser-assisted catalytic growth.

391. (Previously Presented) The method of claim 383, wherein the collection of molecules comprises a cluster of molecules of a catalyst material.

392. (Previously Presented) The method of claim 391, wherein act (A) comprises:
controlling a width of the semiconductor.

393. (Previously Presented) The method of claim 392, wherein controlling the width of the semiconductor comprises:
controlling a width of the catalyst cluster.

394. (Previously Presented) The method of claim 378, wherein act (A) further comprises:
performing chemical vapor deposition on at least the molecules.

395. (Previously Presented) The method of claim 378, wherein the grown semiconductor has at least one portion having a smallest width of less than 20 nanometers.

396. (Previously Presented) The method of claim 395, wherein the grown semiconductor has at least one portion having a smallest width of less than 10 nanometers.

397. (Previously Presented) The method of claim 395, wherein the grown semiconductor has at least one portion having a smallest width of less than 5 nanometers.

398. (Previously Presented) The method of claim 378, wherein the grown semiconductor is magnetic.

399. (Previously Presented) The method of claim 398, wherein act (A) comprises:
doping the semiconductor with a material that makes the grown semiconductor magnetic.

400. (Previously Presented) The method of claim 378, wherein the grown semiconductor is ferromagnetic.

401. (Previously Presented) The method of claim 400, act (A) comprises:

doping the semiconductor with a material that makes the grown semiconductor ferromagnetic.

402. (Previously Presented) The method of claim 401, wherein act (A) comprises:

doping the semiconductor with manganese.

403. (Previously Presented) A method of fabricating a device, comprising an act of:

(A) contacting one or more semiconductors to a surface, wherein at least one of the semiconductors is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers.

404. (Previously Presented) The method of claim 403, wherein the surface is a substrate.

405. (Previously Presented) The method of claim 403, further comprising an act of:

(B) prior to act (A), growing at least one of the semiconductors by applying energy to molecules of a semiconductor and molecules of a dopant.

406. (Previously Presented) The method of claim 403, wherein act (A) comprises:

contacting a solution comprising the one or more semiconductors to the surface.

407. (Previously Presented) The method of claim 406, further comprising:

(B) aligning one or more of the semiconductors on the surface using an electric field.

408. (Previously Presented) The method of claim 407, wherein act (B) comprises:

generating an electric field between at least two electrodes; and

positioning one or more of the semiconductors between the electrodes.

409. (Previously Presented) The method of claim 406, further comprising an act of:

(B) repeating act (A) with another solution comprising one or more other semiconductors, wherein at least one of the other semiconductors is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers.

410. (Previously Presented) The method of claim 403, further comprising an act of:

(B) conditioning the surface to attach the one or more contacted semiconductors to the surface.

411. (Previously Presented) The method of claim 410, wherein act (B) comprises:

forming channels on the surface.

412. (Previously Presented) The method of claim 410, wherein act (B) comprises:

patterning the surface.

413. (Previously Presented) The method of claim 403, further comprising:

(B) aligning one or more of the semiconductors on the surface using an electric field.

414. (Previously Presented) The method of claim 413, wherein act (B) comprises:

generating an electric field between at least two electrodes; and

positioning one or more of the semiconductors between the electrodes.

415. (Previously Presented) A method of generating light, comprising an act of:

(A) applying energy to one or more semiconductors causing the one or more semiconductors to emit light, wherein at least one of the semiconductors is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a

free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers.

416. (Previously Presented) The method of claim 415, wherein the semiconductor comprises a direct-band-gap semiconductor.

417. (Previously Presented) The method of claim 415, wherein act (A) comprises applying a voltage across a junction of two crossed semiconductors, each semiconductor having a smallest width of less than 500 nanometers.

418. (Previously Presented) The method of claim 417, wherein each semiconductor has a smallest width of less than 100 nanometers.

419. (Previously Presented) The method of claim 415, further comprising an act of:

(B) controlling a wavelength of the emitted light by controlling a dimension of the at least one semiconductor having a smallest width of less than 100 nanometers.

420. (Previously Presented) The method of claim 419, wherein the semiconductor is elongated, and act (B) comprises:

controlling a width of the elongated semiconductor.

421. (Previously Presented) The method of claim 419, wherein:

the semiconductor has a property that a mass of the semiconductor emits light at a first wavelength if the mass has a minimum shortest dimension, and

the controlled dimension of the semiconductor is less than the minimum shortest dimension.

422. (Previously Presented) A method of fabricating a device having a doped semiconductor component and one or more other components, the method comprising acts of:

(A) doping a semiconductor during its growth to produce the doped semiconductor component; and

(B) attaching the doped semiconductor component to at least one of the one or more other components.

423. (Previously Presented) The method of claim 422, wherein the doped semiconductor component is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers.

424. (Previously Presented) A process for controllably assembling a semiconductor device having elongated elements with a characteristic dimension in a transverse direction of the element on a nanometer scale, comprising:

producing at least one first element of a first doping type,

orienting said first element in a first direction, and

connecting said first element to at least one first contact to allow an electrical current to flow through the first element.

425. (Previously Presented) The process of claim 424, further comprising:

producing at least one second element of a second doping type,

orienting said second element in a second direction different from the first direction,

enabling an electrical contact between the first element and the second element, and

connecting said second element to at least one second contact to allow an electrical current to flow between the first and second element.

426. (Previously Presented) The process of claim 425, wherein the second doping type is n-type if the first doping type is p-type, and p-type if the first doping type is n-type.

427. (Previously Presented) The process of claim 425, wherein the second element is oriented by applying at least one of an electric field or a fluid flow.

428. (Previously Presented) The process of claim 424, further comprising:

connecting said first element to spaced-apart contacts and arranging a gate electrode proximate to the first element between the spaced-apart contacts, thereby forming an FET.

429. (Previously Presented) The process of claim 424, wherein the semiconductor device is made of a material selected from the group consisting of Si, Ge, Sn, Se, Te, B, Diamond, P, B-C, B-P(BP_6), B-Si, Si-C, Si-Ge, Si-Sn and Ge-Sn, SiC, BN/BP/BAs, AlN/AlP/AlAs/AlSb, GaN/GaP/GaAs/GaSb, InN/InP/InAs/InSb, BN/BP/BAs, AlN/AlP/AlAs/AlSb, GaN/GaP/GaAs/GaSb, InN/InP/InAs/InSb, ZnO/ZnS/ZnSe/ZnTe, CdS/CdSe/CdTe, HgS/HgSe/HgTe, BeS/BeSe/BeTe/MgS/MgSe, GeS, GeSe, GeTe, SnS, SnSe, SnTe, PbO, PbS, PbSe, PbTe, CuF, CuCl, CuBr, CuI, AgF, AgCl, AgBr, AgI, $BeSiN_2$, $CaCN_2$, $ZnGeP_2$, $CdSnAs_2$, $ZnSnSb_2$, $CuGeP_3$, $CuSi_2P_3$, (Cu, Ag)(Al, Ga, In, Tl, Fe)(S, Se, $Te)_2$, Si_3N_4, Ge_3N_4, Al_2O_3, (Al, Ga, $In)_2$(S, Se, $Te)_3$, and Al_2CO.

430. (Previously Presented) The process of claim 424, wherein the first doping type is one of n-type or p-type.

431. (Previously Presented) The process of claim 424, wherein the first element is oriented by applying at least one of an electric field or a fluid flow.

432. (Previously Presented) The process of claim 431, wherein the first element is suspended in the fluid flow.

433. (Previously Presented) The process of claim 424, wherein the first element is oriented by applying a mechanical tool.

434. (Previously Presented) The process of claim 424, wherein the second element is suspended in the fluid flow.

435. (Previously Presented) The process of claim 424, wherein the second element is oriented by applying a mechanical tool.

436. (Previously Presented) A method for manufacturing a nanowire semiconductor device comprising positioning a first nanowire between two contact points by applying a potential between the contact points; and positioning a second nanowire between two other contact points.

437. (Previously Presented) A method for manufacturing a nanowire semiconductor device comprising forming a surface with one or more regions that selectively attract nanowires.

438. (Previously Presented) A method for manufacturing a light-emitting diode from nanowires, the diode having an emission wavelength determined by a dimension of a p-n junction between two doped nanowires.

439. (Previously Presented) A method for manufacturing a semiconductor junction by crossing a p-type nanowire and an n-type nanowire.

440. (Previously Presented) A method of assembling one or more elongated structures on a surface, the method comprising acts of:

(A) flowing a fluid that comprises the one or more elongated structures onto the surface; and

(B) aligning the one or more elongated structures on the surface to form an array of the elongated structures.

441. (Previously Presented) The method of claim 440, wherein act (A) comprises flowing the fluid in a first direction and act (B) comprises aligning the one or more elongated structures as the fluid flows in the first direction to form a first layer of arrayed structures, and wherein the method further comprises:

(C) changing a direction of the flow from the first direction to a second direction; and

(D) repeating acts (A) and (B) in the second direction to form a second layer of arrayed structures.

442. (Previously Presented) The method of claim 441, comprising repeating acts (C) and (D) one or more times.

443. (Previously Presented) The method of claim 441, wherein at least a first elongated structure from the first layer contacts at least a second elongated structure from the second array.

444. (Previously Presented) The method of claim 443, wherein one of the first and second elongated structures is doped semiconductor of a first conductivity type and another of first and second elongated structures is doped semiconductor of a second conductivity type.

445. (Previously Presented) The method of claim 444, wherein the first conductivity type is p-type and the second conductivity type is n-type, and wherein the first and second elongated structures form a p-n junction.

446. (Previously Presented) The method of claim 440, wherein the surface is a surface of a substrate.

447. (Previously Presented) The method of claim 446, wherein the method further comprises:

(C) transferring the array of elongated structures from the surface of the substrate to a surface of another substrate.

448. (Previously Presented) The method of claim 447, wherein act (C) comprises stamping.

449. (Previously Presented) The method of claim 440, wherein the one or more elongated structured are aligned onto the surface while still comprised in the fluid.

450. (Previously Presented) The method of claim 440, wherein the method further comprises:

(C) conditioning the surface with one or more functionalities that attract the one or more elongated structures to particular positions on the surface,

wherein act (B) comprises attracting the one or more elongated structures to the particular positions using the one or more functionalities.

451. (Previously Presented) The method of claim 450, wherein act (C) comprises:
conditioning the surface with one or more molecules.

452. (Previously Presented) The method of claim 450, wherein act (C) comprises:
conditioning the surface with one or more charges.

453. (Previously Presented) The method of claim 450, wherein act (C) comprises:
conditioning the surface with one or more magnetos.

454. (Previously Presented) The method of claim 450, wherein act (C) comprises:
conditioning the surface with one or more light intensities.

455. (Previously Presented) The method of claim 450, wherein act (C) comprises:
conditioning the surface with one or more functionalities that attract the one or more elongated structures to particular positions on the surface using chemical force.

456. (Previously Presented) The method of claim 450, wherein act (C) comprises:
conditioning the surface with one or more functionalities that attract the one or more elongated structures to particular positions on the surface using optical force.

457. (Previously Presented) The method of claim 450, wherein act (C) comprises:
conditioning the surface with one or more functionalities that attract the one or more elongated structures to particular positions on the surface using electrostatic force.

458. (Previously Presented) The method of claim 450, wherein act (C) comprises:
conditioning the surface with one or more functionalities that attract the one or more elongated structures to particular positions on the surface using magnetic force.

459. (Previously Presented) The method of claim 440, wherein the method further comprises:

(C) patterning the surface to receive the one or more elongated structures at particular positions on the surface.

460. (Previously Presented) The method of claim 459, wherein act (C) comprises:
creating physical patterns on the surface.

461. (Previously Presented) The method of claim 460, wherein the physical patterns are trenches.

462. (Previously Presented) The method of claim 460, wherein the physical patterns are steps.

463. (Previously Presented) The method of claim 460, wherein the surface is a surface of a substrate, and wherein creating physical patterns on the surface comprises:
using crystal lattice steps of the substrate.

464. (Previously Presented) The method of claim 460, wherein the surface is a surface of a substrate, and wherein creating physical patterns on the surface comprises:
using self-assembled di-block polymer strips.

465. (Previously Presented) The method of claim 460, wherein creating physical patterns on the surface comprises:
using patterns.

466. (Previously Presented) The method of claim 465, wherein creating physical patterns on the surface comprises:
using imprinted patterns.

467. (Previously Presented) The method of claim 440, wherein act (A) comprises controlling the flow of the fluid using a channel.

468. (Previously Presented) The method of claim 440, wherein at least one of the elongated structures are semiconductors.

469. (Previously Presented) The method of claim 440, wherein at least one of the elongated structures are doped semiconductors.

470. (Previously Presented) The method of claim 469, wherein at least one of the elongated structures are bulk-doped semiconductors.

471. (Previously Presented) The method of claim 440, wherein at least one of the structures is a doped single-crystal semiconductor.

472. (Previously Presented) The method of claim 440, wherein at least one of the structures is an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers.

473. (Previously Presented) The method of claim 440, wherein at least one of the structures is a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers.

474. (Previously Presented) The method of claim 440, wherein at least one of the structures is a doped semiconductor that is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers.

475. (Previously Presented) The method of claim 474, wherein the doped semiconductor comprises a semiconductor selected from a group consisting of: Si, Ge, Sn, Se, Te, B, Diamond, P, B-C, B-P(BP_6), B-Si, Si-C, Si-Ge, Si-Sn and Ge-Sn, SiC, BN/BP/BAs, AlN/AlP/AlAs/AlSb, GaN/GaP/GaAs/GaSb, InN/InP/InAs/InSb, BN/BP/BAs, AlN/AlP/AlAs/AlSb, GaN/GaP/GaAs/GaSb, InN/InP/InAs/InSb, ZnO/ZnS/ZnSe/ZnTe, CdS/CdSe/CdTe,

HgS/HgSe/HgTe, BeS/BeSe/BeTe/MgS/MgSe, GeS, GeSe, GeTe, SnS, SnSe, SnTe, PbO, PbS, PbSe, PbTe, CuF, CuCl, CuBr, CuI, AgF, AgCl, AgBr, AgI, $BeSiN_2$, $CaCN_2$, $ZnGeP_2$, $CdSnAs_2$, $ZnSnSb_2$, $CuGeP_3$, $CuSi_2P_3$, (Cu, Ag)(Al, Ga, In, Tl, Fe)(S, Se, Te)$_2$, Si_3N_4, Ge_3N_4, Al_2O_3, (Al, Ga, In)$_2$(S, Se, Te)$_3$, and Al_2CO.

476. (Previously Presented) The method of claim 474, wherein the doped semiconductor comprises a dopant selected from a group consisting of: a p-type dopant from Group III of the periodic table; an n-type dopant from Group V of the periodic table; a p-type dopant selected from a group consisting of: B, Al and In; an n-type dopant selected from a group consisting of: P, As and Sb; a p-type dopant from Group II of the periodic table; a p-type dopant selected from a group consisting of: Mg, Zn, Cd and Hg; a p-type dopant from Group IV of the periodic table; a p-type dopant selected from a group consisting of: C and Si.; and an n-type is selected from a group consisting of: Si, Ge, Sn, S, Se and Te.

477. (Previously Presented) The method of claim 474, wherein the doped semiconductor is doped during growth of the semiconductor.

478. (Previously Presented) A method of assembling one or more elongated structures on a surface, wherein one or more of the elongated structures are at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers, and wherein the method comprises acts of:

(A) conditioning the surface with one or more functionalities that attract the one or more elongated structures to particular positions on the surface, and

(B) aligning the one or more elongated structures by attracting the one or more elongated structures to the particular positions using the one or more functionalities.

479. (Previously Presented) The method of claim 478, wherein act (A) comprises:

conditioning the surface with one or more molecules.

480. (Previously Presented) The method of claim 478, wherein act (A) comprises:
conditioning the surface with one or more charges.

481. (Previously Presented) The method of claim 478, wherein act (A) comprises:
conditioning the surface with one or more magnetos.

482. (Previously Presented) The method of claim 478, wherein act (A) comprises:
conditioning the surface with one or more light intensities.

483. (Previously Presented) The method of claim 478, wherein act (A) comprises:
conditioning the surface with one or more functionalities that attract the one or more elongated structures to particular positions on the surface using chemical force.

484. (Previously Presented) The method of claim 478, wherein act (A) comprises:
conditioning the surface with one or more functionalities that attract the one or more elongated structures to particular positions on the surface using optical force.

485. (Previously Presented) The method of claim 478, wherein act (A) comprises:
conditioning the surface with one or more functionalities that attract the one or more elongated structures to particular positions on the surface using electrostatic force.

486. (Previously Presented) The method of claim 478, wherein act (A) comprises:
conditioning the surface with one or more functionalities that attract the one or more elongated structures to particular positions on the surface using magnetic force.

487. (Previously Presented) A method of assembling a plurality of elongated structures on a surface, wherein one or more of the elongated structures are at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers, and wherein the method comprises acts of:

(A) depositing the plurality of elongated structures onto the surface; and

(B) electrically charging the surface to produce electrostatic forces between two or more of the plurality of the elongated structures.

488. (Previously Presented) The method of claim 487, wherein the electrostatic forces cause the two or more elongated structures to align themselves.

489. (Previously Presented) The method of claim 488, wherein the electrostatic forces cause the two or more elongated structures to align themselves into one or more patterns.

490. (Previously Presented) The method of claim 489, wherein the one or more patterns comprise a parallel array.

491. (Previously Presented) A method of assembling a plurality of elongated structures on a surface, wherein one or more of the elongated structures are at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers, and wherein the method comprises acts of:

(A) dispersing the one or more elongated structures on a surface of a liquid phase to form a Langmuir-Blodgett film;

(B) compressing the Langmuir-Blodgett film; and

(C) transferring the compressed Langmuir-Blodgett film onto a surface.

492. (Previously Presented) The method of claim 491, wherein the surface is the surface of a substrate.

493. (Previously Presented) A method of assembling a plurality of one or more elongated structures on a surface, wherein at least one of the elongated structures are at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a

free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers, and wherein the method comprises acts of:

(A) dispersing the one or more elongated structures in a flexible matrix;

(B) stretching the flexible matrix in a direction to produce a shear force on the one or more elongated structures that causes the at least one elongated structure to align in the direction;

(C) removing the flexible matrix; and

(D) transferring the at least one aligned elongated structure to a surface.

494. (Previously Presented) The method of claim 493, wherein the direction is parallel to a plane of the surface.

495. (Previously Presented) The method of claim 493, wherein act (B) comprises: stretching the flexible matrix with an electrically-induced force.

496. (Previously Presented) The method of claim 493, wherein act (B) comprises: stretching the flexible matrix with an optically-induced force.

497. (Previously Presented) The method of claim 493, wherein act (B) comprises: stretching the flexible matrix with a mechanically-induced force.

498. (Previously Presented) The method of claim 493, wherein act (B) comprises: stretching the flexible matrix with a magnetically-induced force.

499. (Previously Presented) The method of claim 493, wherein the surface is a surface of a substrate.

500. (Previously Presented) The method of claim 493, wherein the flexible matrix is a polymer.